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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

SPITTLE, MATTHEW D

ART UNIT PAPER NUMBER

2111

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/814,106	Applicant(s) JOLLY ET AL.	
	Examiner Matthew D. Spittle	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 18-27 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-17 is/are allowed.
- 6) ☒ Claim(s) 1-9, 18-22, 26 and 27 is/are rejected.
- 7) ☒ Claim(s) 23-25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Page 4, lines 18 and 20 contain misspellings of the word "exist."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 5, 9, 18 – 22, 26, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Gould.

With regard to claim 1, Gould describes a circuit comprising:

A receiver to receive a transfer signal (Figure 17, item 666; where a transfer signal is interpreted as the output of the AND gate (Figure 17, item 664));

A signal detector connected to the receiver (Figure 17, items 666, 656) to generate an internal signal (Figure 17, item 656 output Q'; Figure 18, labeled as Q' OUTPUT OF F/F 656) based on the transfer signal, wherein the signal detector is configured to hold the internal signal at a first signal level (interpreted as a low logic signal) when the transfer signal repeatedly switches between the first signal level and a

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second signal level, and wherein the signal detector is configured to hold the internal signal at the second signal level (interpreted as a logic high) when the transfer signal stops switching (Figure 18).

With regard to claim 2, Gould describes the circuit of claim 1, wherein signal detector includes a detect circuit to detect for changes in voltage levels represented by the transfer signal (Examiner identifies Figure 17 items 666, 656 as the signal detector, and notes that both could be interpreted as including a detect circuit to detect changes in voltage levels since both are responsive to changes in voltage levels).

With regard to claim 3, Gould describes the circuit of claim 2, wherein signal detector further includes a switching circuit to switch the internal signal between the first and second signal levels (Examiner takes official notice that both Figure 17 items 666 and 656 may include transistors as is well known in the art, and therefore comprise switching circuits).

With regard to claim 4, Gould describes the circuit of claim 3, wherein signal detector further includes a holding circuit to hold the internal signal at one of the first and second signals (Examiner identifies that the signal detector (comprised of Figure 17, items 666 and 656) includes a holding circuit as evidenced by the timing diagram of Figure 18 showing the Q' OUTPUT OF F/F 656 being held at both high and low logic levels).

With regard to claim 5, Gould describes an integrated circuit comprising:

A plurality of terminals (column 18, lines 24 – 26);

A number of transmitters connected to the terminals to transmit signals (Figure 16, item 520);

A number of receivers connected to the terminals to receive signals (Figure 17, item 666; where a transfer signal is interpreted as the output of the AND gate (Figure 17, item 664));

A signal detector (Figure 17, items 666, 656) connected to at least one of the receivers to control an internal signal (Figure 17, item 656 output Q'; Figure 18, labeled as Q' OUTPUT OF F/F 656) based on a transfer signal received by one of the receivers, wherein the signal detector is configured to switch the internal signal from a first signal level (interpreted as a logic high) to a second signal level (interpreted as a logic low) when the transfer signal repeatedly switches between the first and second signal levels, and wherein the signal detector is configured to switch the internal signal from the second signal level back to the first signal level when the transfer signal stops switching (Figure 18).

With regard to claim 9, Gould describes the integrated circuit of claim 5 further comprising a transmitting circuit, the transmitting circuit including:

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An input node to receive a send signal (interpreted as SENSE DATA in Figure 17) having the first and second signal levels (Figure 17, item 664; where the first and second signal levels are interpreted as logic low and logic high);

An output node (Figure 17, item 664) to transfer the transfer signal to one of the terminals, wherein the transmitting circuit is configured to hold the transfer signal at one of the first and second signal levels when the send signal has the first signal level (when the SENSE DATA is low, the transfer signal is held at logic high as in Figure 18; where a transfer signal is interpreted as the output of AND gate item 664 in Figure 17), and wherein the transmitting circuit repeatedly switches the transfer signal between the first and second signal levels when the send signal has the second signal level (When the SENSE DATA goes to logic high, the decoder (Figure 17, item 616) input on AND gate item 664 in Figure 17 is passed through to its output as evidenced by Figure 18).

With regard to claim 18, Gould describes a method comprising:

Monitoring a transfer signal (Examiner interprets monitoring to mean “detecting and responding to changes,” and interprets the output of AND gate (Figure 17, item 664) to be a transfer signal. Since OR gate (item 666) responds to changes in the transfer signal, examiner finds it to meet this limitation).

Holding an internal signal (where an internal signal is interpreted as the Q' output of item 656 in Figure 17) at a first signal level (interpreted as a logic high) when the transfer signal stays at one of the first signal level and a second signal level;

Holding the internal signal at a second signal level (interpreted as a logic low) when the transfer signal repeatedly switches between the first and second signal levels (Figure 18, where an internal signal is interpreted as the Q' OUTPUT OF F/F 656);

Switching the internal signal from the second signal level to the first signal level when the transfer signal stops switching (Figure 18, where the transfer signal is interpreted as the SENSE LINE A8, B8, C8 (B8 TOUCHED), and the internal signal is interpreted as the Q' OUTPUT OF F/F 656).

With regard to claim 19, Gould describes the method of claim 18 further comprising:

Holding the internal signal at the first signal level after transfer signal stops switching (Figure 18 evidences this behavior; where the internal signal is interpreted as the Q' OUTPUT OF F/F 656).

With regard to claim 20, Gould describes the method of claim 18, wherein monitoring includes detecting for changes in signal levels of the transfer signal (where the transfer signal may be interpreted as the output of AND gate (Figure 17, item 664). Since OR gate (item 666) responds to changes in the transfer signal, examiner finds it to meet this limitation).

With regard to claim 21, Gould describes the method of claim 18, wherein one of the first signal level and the second signal level represents one of a voltage level and

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ground. Gould implicitly describes this limitation since he teaches that the invention uses digital logic means (Column 1, lines 52 – 60). Examiner takes official notice that it is well known in the art of digital systems to have a first signal level representing some voltage level and a second signal level representing ground.

With regard to claim 22, Gould describes the method of claim 18, wherein the transfer signal (where a transfer signal is interpreted as the output of the AND gate (Figure 17, item 664) is generated based on a send signal (where a send signal may be interpreted as SENSE DATA in Figure 17), wherein each of send signal and the internal signal has a frequency lower than the frequency of the transfer signal (Figure 18 illustrates the frequency of SENSE LINE A8, B8, C8 (B8 TOUCHED) (interpreted as the transfer signal) is higher than either the send signal (interpreted as SENSE DATA in Figure 17) or the internal signal (interpreted as Q' OUTPUT OF F/F 656 in Figure 18)).

With regard to claim 26, Gould describes the method of claim 18, wherein holding the internal signal (Figure 17, item 656 output Q'; Figure 18, labeled as Q' OUTPUT OF F/F 656) at the first signal level (interpreted as a logic high) occurs when the transfer signal (interpreted as SENSE LINE A8, B8, C8 (B8 TOUCHED)) stays at one of the first and second signal levels (interpreted as a logic low) for a time interval equal to at least one cycle of the transfer signal (Figure 18).

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With regard to claim 27, Gould describes the method of claim 26, wherein holding the internal signal (Figure 17, item 656 output Q'; Figure 18, labeled as Q' OUTPUT OF F/F 656) at the second signal level (interpreted as logic low) occurs when the transfer signal (interpreted as SENSE LINE A8, B8, C8 (B8 TOUCHED)) repeatedly switches between the first and second signal level such that the transfer signal has at least two consecutive cycles (Figure 18 shows that Q' OUTPUT OF F/F 656 does not change until SENSE LINE A8, B8, C8 (B8 TOUCHED) has transitioned through two cycles).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould in view of Janus et al.

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With regard to claim 6, Gould fails to teach the transmitters and receivers configured to transfer data via the terminals according to peripheral component interconnect (PCI) express standard.

Janus et al. teach using the peripheral component interconnect express standard (paragraph 19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the PCI express standard as taught by Janus et al. into the invention of Gould for the purpose of transmitting and receiving data on a bus. This would have been obvious since Janus et al. teach that the PCI express architecture has the advantages of low pin count, and high speed, serial device-to-device interconnect.

With regard to claim 7, Gould fails to teach the transmitters and receivers configured to transfer data via the terminals according to serial digital video output (SVDO) standard.

Janus et al. teach using the serial digital video output standard (paragraph 20).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the SVDO standard as taught by Janus et al. into the invention of Gould for the purpose of connecting a display device. This would have been obvious since Janus et al. teach that SVDO devices can generate digital display signals to drive a display monitor (paragraph 23).

With regard to claim 8, Gould fails to teach the transmitters and the receivers configured to transfer data via the terminals according both a peripheral component interconnect (PCI) express standard and a serial digital video output (SDVO) standard.

Janus et al. teach using both a PCI express standard and SDVO standard (paragraphs 19, 20).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate both the PCI express and SDVO standards for the purposes as described above. Additionally, this would have been obvious since Janus et al. teach that SDVO and PCI express signals are physically and electrically compatible (paragraph 28).

Allowable Subject Matter

Claims 23 – 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10 – 17 are allowed.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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1/19/06